REMARKS

Claims 31-50 are pending. Of those, claims 31, 41 and 50 are independent.

Claim Objections

On page 2 of the Office Action, claims 34 and 44 are objected to as containing informalities. More particularly, the Examiner has identified the same two typographical errors in each of dependent claims 34 and 44. Applicant appreciates the Examiner's attentiveness in spotting the problems and has adopted the Examiner's suggested corrections by the amendments of this reply. Withdrawal of the objection is requested.

It is submitted that the present amendments are non-narrowing as they merely correct typographical errors. In other words, the present amendments have not been made to distinguish over prior art.

§102 Rejection

Beginning on page 3 of the Office Action, claims 31-38 and 40-50 are rejected under 35 U.S.C. §102(b) as being anticipated by US Patent No. 4,905,141 to Brenza (the '141 patent). Applicants traverse.

The '141 patent is generally directed toward a memory design that may handle a large number of cache requests in a short time interval or essentially simultaneously; see col. 3, lines 13-16. Applicant acknowledges that the '141 patent is generally directed toward a partitioned cache memory; see col. 3, lines 35-50.

But the '141 is conventional regarding how partitions 50 (Fig.2) of L1 cache 34 (Fig. 1) are allotted. While the '141 patent is disclosed in the context of a system 10 having multiple central processing units (CPUs) 12, 14 and 16 (see col. 5, lines 18-20), it

should be noted that the cache memory design representing the invention of the '141 patent concerns L1 cache 34 included within each of CPUs 12, 14 and 16; see col. 5, lines 43-46.

Each one of CPUs includes plural central processor logical units (CPLUs) 70-76; see col. 6, lines 47-51, and col. 7, lines 9-10. It will be assumed for the sake of argument that the plurality of CPLUs 70-74 correspond to a plurality of processors, and that L1 cache 34 is an appropriate level of cache for the discussion.

The '141 patent incorporates U.S. Patent No. 4,843,541 by reference. And the Examiner discusses the '541 patent as if it were a part of the disclosure of the '141 patent. It further will be assumed that the Examiner's discussion of the '541 patent is appropriate in the context of a §102 rejection. It is noteworthy that, of its 60 columns, Applicant's review of the '541 patent finds that it mentions the term "cache" only once; see col. 25, line 4.

Each of CPLUs 70-76 of the '141 patent can access any and/or all of the partitions 50 (see Fig. 2) of L1 cache 50, which is conventional. The '141 patent is silent about there being any other arrangement, e.g., some of CPLUs 70-76 not having access to all of partitions 50 of L1 cache 34, etc. Each one of CPLUs 70-76 has a corresponding one of partition look-aside tables (PLATs) 100-108. The Examiner has asserted that PLATs 100-108 correspond to the plurality of tables recited in present claim 1; Applicant disagrees.

PLATs 100-108 merely are provided to enhance the speed with which a cache "hit" or cache "miss" is determined. Each PLAT corresponds to one of the partitions 50 of L1 cache 34. A given one of PLATs 100-108 is checked to determine if the corresponding partition has the desired cache line, and, if not, then a global cache check is made for the desired cache line; see col. 4, lines 9-16. A given one of PLATs 100-108,

e.g., 100, do not identify which ones of partitions 50 of L1 cache 34 are available to CPLU, e.g., 70, because it is assumed that all of partitions 50 are available to CPLU 70.

A distinction of independent claim 1 over the '141 patent is that each of the plurality of tables respectively identifies which of the plurality of cache units are available to the corresponding processor. Again, the disclosed PLATs 100-108 of the '141 patent does not store such information because each of partitions 50 of L1 cache 34 is available to each of CPLUs 101-108.

Claims 32-38 and 40 depend at least indirectly from claim 31 and, as such, exhibit at least the same distinction, respectively.

Each of independent claims 41 and 50 recites features that are similar to those of claim 1, and thus each of claims 41 and 50 similarly distinguishes over the '141 patent, respectively. Claims 42-49 depend at least indirectly from claim 31 and, as such, exhibit at least the same distinction, respectively.

In view of the foregoing discussion, the §102(b) rejection of claims 31-38 and 40-50 over the '141 patent is improper. Withdrawal of the rejection is requested.

§103 Rejection

Beginning on page 7 of the Office Action, claim 39 is rejected under 35 U.S.C. §103(a) as being obvious over the '141 patent in view of the Olukotun reference (Kunle Olukotun et al, "The Case for a Single-Chip Multiprocessor). Applicants traverse.

Claim 39 depends from claim 1 and, as such, exhibits at least the distinction of claim (noted above) over the '141 patent. The Olukotun reference fails to make up for the shortcomings of the '141 patent.

Thus, the §103(a) rejection of claim 39 as being obvious over the '141 patent in view of the Olukotun reference is improper. Withdrawal of the rejection is requested.

CONCLUSION

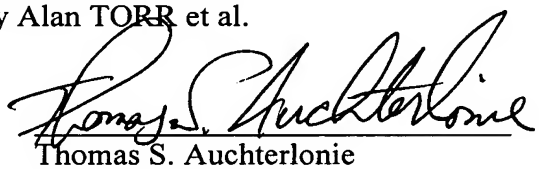
The issues in the case are considered to be resolved. Accordingly, Applicant again requests a Notice of Allowability.

Person to Contact

In the event that any matters remain at issue in the application, the Examiners are invited to contact the undersigned at (703) 668-8000 in the Northern Virginia area, for the purpose of a telephonic interview.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-2025 for any additional fees under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Respectfully submitted,
Terry Alan TORR et al.

By: 
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